In the Specification:

Please replace paragraph **[0013]** with the following amended paragraph:

-- **[0013]** Referring to Fig. 2A, an element isolation oxide layer, e.g. a shallow trench isolation (STI) 2 is thermally grown on a silicon substrate 1 to an isolation depth. A first nitride layer 3 is then deposited on the element isolation oxide layer 2. A first photoresist (not shown) is then patterned using the element isolation mask 100. The first nitride layer 3 and the element isolation oxide layer 2 are sequentially etched by an anisotropic dry etching process to thereby expose the silicon substrate 1 in a portion where an active region is formed. Thereafter, the first photoresist is removed and a cleaning process for the silicon substrate 1 is performed. Next, an epitaxial active region 4 is epitaxially grown on the silicon substrate 1. A first oxide layer 5 is then deposited on the epitaxial active region 4 to a thickness of a gate electrode to be formed later. A second photoresist 6 is patterned using the source/drain mask 200. The first oxide layer 5 is then etched by the anisotropic dry etching process. At this time, the first oxide layer 5 is not entirely removed and remains with a predetermined thickness. In Fig. 2A, L is a width between a source and a drain so that L is a channel length of the gate electrode to be formed later.--.

Please replace paragraph **[0019]** with the following amended paragraph:

-- **[0019]** Referring to Fig. 2E, the third photoresist 9 is removed. Then a ~~second~~ third nitride layer 10 is deposited on the overall surface and etched back. By doing this, the ~~second~~ third nitride layer 10 for use in controlling the length of the gate remains at a predetermined thickness, e.g., l. Next, a local channel 11 is ion-implanted. Then a gate insulation layer 12 and a gate electrode 13 are sequentially deposited on the active region 4. Thereafter, the gate electrode 13 is planarized. A second oxide layer 14 is then thickly deposited. A gate electrode plug 15a, a source electrode plug 15b and a drain electrode plug 15c are then formed.--.

Please replace paragraph **[0020]** with the following amended paragraph:

-- **[0020]** From the foregoing, persons of ordinary skill in the art will appreciate that a gate having a fine pattern can be formed by using the ~~second~~ third nitride layer 10 to control the channel length of the gate. Thus, new methods capable of enhancing an operating characteristic of a transistor and reducing a cost of a lithography tool are provided.--.